BAPVC Annual Project Report

Project Title: Novel Interconnects
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Summary:

The goal of developing novel interconnects is to monolithically interconnect PV cells in modules employing a single pass process after the deposition of all layers while simultaneously reducing dead zone area. Printed interconnects have been made for CIGS and CdTe using aerosol jet printing of dielectric and metal inks in conjunction with laser and mechanical scribing. Architectures using a 3-scribe and 2-scribe method were developed with best results obtained using PMMA (dielectric) and NovaCentrix Silver Nano-crystalline (metal) Inks.

Key Accomplishments:

The monolithic interconnect architecture serves to electronically isolate the top and bottom electrodes in the P1 scribe, as shown in Fig. 1. Fig. 1(b) and Fig. 1(c) show the alternative architectures of the 3-scribe and 2-scribe methods, respectively. Each method was constructed using laser-scribing via pulsed YAG at 1064 nm for P1 scribes and mechanical-scribing with a tungsten-carbide tip on an actuated scriber for P2 and optional P3 scribe through the full solar cell stack. Dielectric material, poly(methyl methacrylate) (PMMA), and metallization with NovaCentrix silver nano-crystalline ink were deposited using an aerosol jet system with a substrate temperature of 100°C and 150°C, respectively. An actuated mechanical scribing station was added to the printing station, eliminating the need for alignment between scribing and printing.

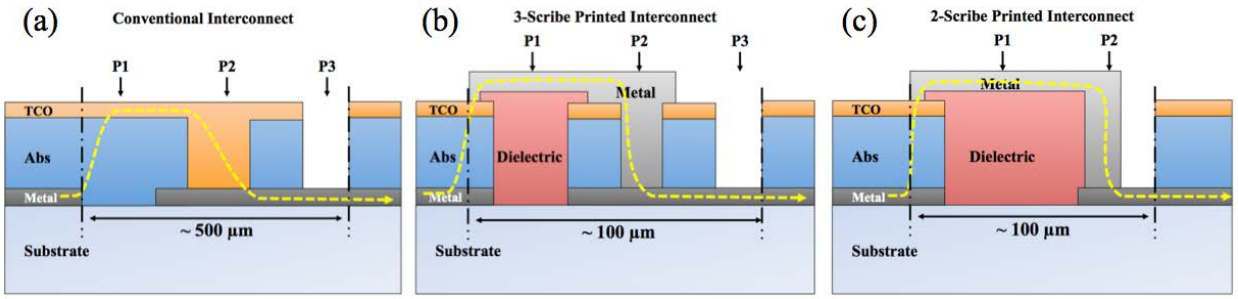
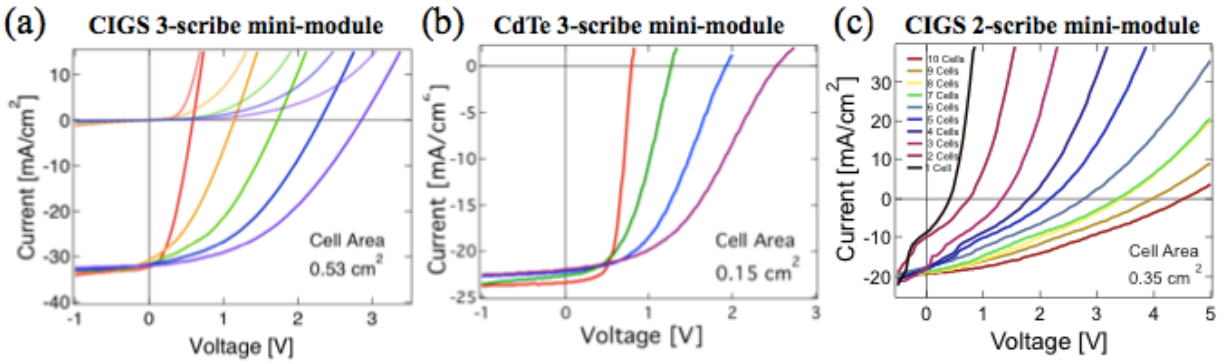


Figure 1: (a) Conventional, (b) 3-scribe printed, and (c) 2-scribe printed interconnect architectures. Cross-sections are labeled with the scribe numbers of P1, P2, and P3 for separation of bottom electrode, top electrode, and next cell, respectively. Areas between the black vertical bars represent the dead zones, which do not contribute to the power production of the cell. The yellow path represents current flow needed for voltage addition.

The 3-scribe printed interconnects were demonstrated for CIGS and CdTe mini-modules. CIGS 3-scribe mini-module J-V traces, shown in Fig. 2 (a), produced near perfect voltage addition for five cells, with minimal current loss or degradation of fill factor. Similarly Fig. 2 (b) presents the

CdTe 3-scribe mini-module where three out of four cells have voltage addition with steady current and fill factors. With the demonstration of proof of concept and identification of compatible materials for printed interconnects, focus shifted to the 2-scribe method in order to minimize the dead zone area. CIGS 2-scribe mini-modules demonstrate good voltage addition of seven out of the ten cells connected, with each drop in current and fill factor corresponding to an addition of a shorted cell. Printed interconnects using the 2-scribe method produce interconnects with widths smaller than 250 µm. With additional optimization 100 µm widths using current equipment is feasible. Cost modeling of the novel printed interconnect shows that the manufacturing costs of a 14% CIGS module can be reduced by 3 cents/W_p.



Cells	Voc		Jsc	FF	PCE
#	V	ΔV	mA/cm2	%	%
1	0.59	0.59	32.3	38.8	8.70
2	1.15	0.56	30.8	35.8	7.45
3	1.73	0.58	31.7	39.1	8.40
4	2.30	0.57	31.7	41.6	8.93
5	2.86	0.56	32.0	42.9	9.24

Cells	Voc		Jsc	FF	PCE
#	V	ΔV	mA/cm2	%	%
1	0.80	0.80	23.4	61.1	11.50
2	1.28	0.48	22.6	48.3	6.70
3	1.93	0.65	22.2	44.5	6.37
4	2.53	0.60	22.0	43.3	6.03

Cells	Voc		Jsc	FF	PCE
#	V	ΔV	mA/cm2	%	%
1	0.42	0.42	8.80	32.6	1.20
2	0.77	0.35	5.00	31.3	1.20
3	1.35	0.58	5.93	25.8	2.07
4	1.82	0.47	4.46	27.3	2.22
5	2.19	0.37	3.64	27.1	2.16
6	2.79	0.60	2.95	29.0	2.38
7	3.39	0.60	2.69	28.4	2.59
8	3.43	0.05	2.39	30.9	2.53
9	3.99	0.56	2.10	23.4	2.60
10	4.56	0.56	1.94	33.1	2.93

Figure 2: J-V traces showing voltage addition from (a) CIGS 3-scribed, (b) CdTe 3-scribed, and (c) CIGS 2-scribe printed interconnects with corresponding open circuit voltage, short-circuit current density, fill factor, and efficiency. CIGS 3-scribed interconnects demonstration successful connection of 5 cells with perfect voltage addition. Four cells on CdTe were connected using the 3-scribed method. CIGS 2-scribe interconnects demonstrated 10 cells connected in series with clear voltage addition.

Future Work:

For the remainder of the project, work focuses on identifying causes for shorts that are formed during the printing of monolithic interconnects. This information will improved the yield and enable the reduction of the interconnect width (<100 µm). To identify causes of shorts and other defects, DLIT, EL, and PL are used throughout the full process of printing the interconnects. Once the printing conditions are optimized, the monolithic interconnect will be applied to CIGS materials with high efficiency (>15%). Finally the work will be summarized in a manuscript that will be submitted for publication in a peer reviewed journal. Continued effort is made to acquire additional funding for this project.