Thrust: Silicon Absorbers and Cells

Grand Challenges and Key Problems

Silicon-based solar cells are the dominant PV technology today with more than 80% market share. The US Department of Energy has set a cost target of $1/W for installed systems to reach parity with other conventional energy sources. While the Si cost component has been decreasing steadily (from over 40% to 19% over the last decade) due to advances in polysilicon and manufacturing scale up, it is still one of the significant cost adders at the module level. Further, the industry is still pushing for thinner Si cells to reduce the module cost further and to leverage the potential higher efficiency and form factor to reduce balance-of-system costs. In this thrust, the key problems which are being addressed to enable high volume manufacturing of high efficiency Si cells are listed below:

1) Commercially viable manufacturing of thin crystalline Si below 50um:
2) Passivation of thin crystalline Si to meet the high efficiency targets
3) Absorption of all available light within a reduced absorber volume
4) Metallization and packaging of thin Si cells into lightweight modules

Existing Projects in our Thrust

The projects in this thrust are targeting one or more of the above mentioned key problems, as described below and shown in figure 1.

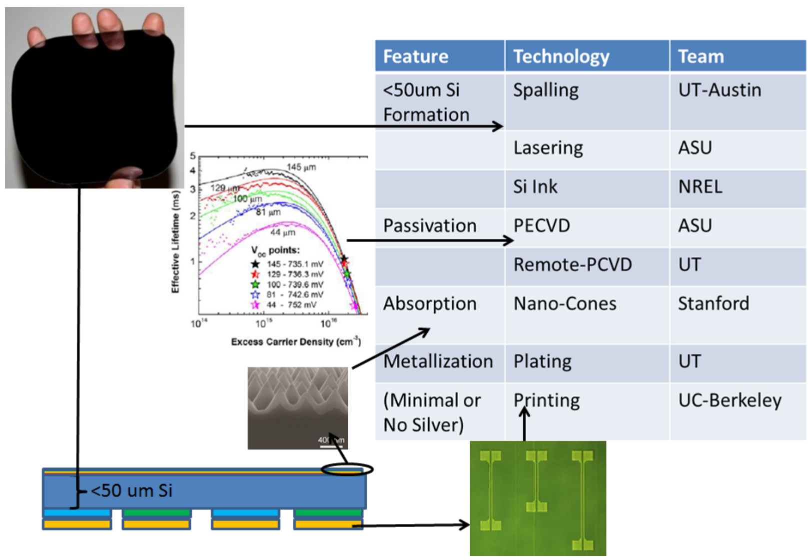
1) Fabrication of 50um thin crystalline Si: Three projects – at Stanford, ASU and at UT-Austin - are addressing this key problem. Stanford is looking at the ultra-thin limit (few microns) to study the physics of enhanced absorption using nanocones at this scale. At ASU, a sub-surface lasering approach is being used to create a weak layer below the Si surface while preserving crystallinity in the top layer. This top layer is then peeled off from the substrate. At University of Texas, a mechanical exfoliation process is being used to spall 30-50um thin Si backed by a metal that makes it robust and handlable. While both these processes hold promise, there are significant challenges in each of them for commercialization. As one possible new initiative, it is proposed to combine the complementary aspects of these two technologies to develop a scalable fabrication process for thin crystalline Si formation. The lasering process can be used for crack initiation at the wafer edges and the spalling process can be used to propagate sub-surface cracks and peel off the crystalline Si layer from the top of the wafer.

2) Passivation of thin crystalline Si: This is a key challenge that needs to be addressed to leverage the potential benefit of higher efficiencies with thin Si. ASU has a PECVD a-Si process for passivation of Si surface that has yielded Voc in excess of 750mV. UT-Austin is developing remote plasma CVD (RPCVD) a-Si processes to complement this effort. It is expected that further optimization is needed for these passivation layers to be useful on thin crystalline Si foils and on nano-cones and other textured surfaces.

3) Light trapping in thin crystalline Si: A key challenge is to absorb all the light that is incident on the surface in a smaller volume of Si compared to regular thick Si cells. One of the approaches being evaluated in this thrust at Stanford is the fabrication of nano-cones of Si on the front surface using a colloidal lithographic process followed by a reactive ion etch. Substantial work needs to be done to

integrate this process on thin crystalline Si foils, especially to improve the effectiveness of surface passivation with nanocones. Low-cost nanoimprint lithography can be used to pattern such nanostructures.

4) Metallization of thin crystalline Si cells: Another challenge to commercialization of thin crystalline Si devices is the ability to effectively metallize flexible thin crystalline cells with low contact resistance and eliminating silver processes. University of California, Berkeley is developing a Cu/Ag alloy nanoparticle based ink to that is resistant to oxidation and Gravure printing as a replacement for traditional Ag printed contacts in Si solar cells. This process allows for printing on flexible substrates and has shown capability to print 2um features. Further work needs to be done to optimize this printing on thin Si foils.



Feature	Technology	Team
<50um Si Formation	Spalling	UT-Austin
	Lasering	ASU
	Si Ink	NREL
Passivation	PECVD	ASU
	Remote-PCVD	UT
Absorption	Nano-Cones	Stanford
Metallization	Plating	UT
(Minimal or No Silver)	Printing	UC-Berkeley

Figure 1: Overview of current projects in this thrust.

Potential Growth of BAPVC

Proposed additional work to accelerate development of these technologies includes:
(a) Processes for thin Si absorber preparation, such as;

- combining the strengths of lasering and spalling approaches to initiate spalling with the lasering process and control thickness uniformity of the spalled Si.
- applying novel thin film formation methods on non-epi substrates (e.g. metal-induced-crystallization) to thin film silicon photovoltaics.

(b) Methods for nano-texturing on thin Si surfaces including colloidal lithography and nano-imprint.
(c) Improved passivation of thin crystalline Si foils which are backed by a supporting substrate using a low temperature process.
(d) Gravure printing on thin Si foils.
(e) Development and sourcing of liquid precursors for silicon and metal films